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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,460	10/27/2003	Hideaki Niimi	M1071.1873	2937

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EXAMINER	
MAYES, MELVIN C	

ART UNIT	PAPER NUMBER
1734	

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,460	NIIMI, HIDEAKI	
	Examiner	Art Unit	
	Melvin Curtis Mayes	1734	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 5-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 5-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/635,818.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/27/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

(1)

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

(2)

Claims 5, 20, 21, 23, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 6-151103 in view of Dirstine 4,386,985.

JP 6-151103 discloses a method of making a laminated semiconductor constituent having positive resistance temperature comprising: forming a mixture including $BaCO_3$ (barium compound) and TiO_2 (titanium compound); baking (calcining) to form a semiconductive barium titanate powder (calcined product); forming semiconductor ceramic layers (ceramic green sheet) from slurry containing the powder; applying nickel-Pd paste on the ceramic layers to form internal electrodes; laminating the ceramic layers; baking in a reducing atmosphere; re-oxidizing; and forming external electrodes on the sintered body (computer translation). JP 6-151103 does not disclose providing a nickel compound in the mixture to be baked (calcined) to form the semiconductive barium titanate powder.

Dirstine teach that in manufacturing a ceramic capacitor from a barium titanate composition and nickel electrodes, the addition of nickel oxide in amounts of about 1 to 2 mol% to the composition optimizes the dielectric properties, in particular the room temperature dielectric constant, and maintains the integrity of the nickel electrodes co-fired with the green ceramic by preventing dissolution and degradation of the nickel electrodes. The nickel oxide (NiO) is added to the composition by mixing with the $BaCO_3$ and TiO_2 and calcining (col. 3, lines 29-40, col. 8, line 26 – col. 9, line 22).

It would have been obvious to one of ordinary skill in the art to have modified the method of JP '103 for making a laminated barium titanate semiconductor constituent having nickel internal electrodes by also providing nickel oxide (nickel compound) in the mixture with

the barium compound and titanium compound to be calcined to form the powder, as taught by Dirstine, to optimize the dielectric properties, in particular the room temperature dielectric constant, and to maintain the integrity of the nickel electrodes co-fired with the green ceramic by preventing dissolution and degradation of the nickel electrodes.

(3)

Claims 6, 7 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the references as applied to claim 5 above, and further in view of JP 11-12033.

JP 11-12033 teaches that boron oxide is added to barium titanate semiconductor composition to lower the sintering temperature of the composition and to provide particle growth of uniform particle size by liquid phase sintering. Boron oxide is added to the BaCO3 and TiO2 before calcining so that the calcined composition contains 0.3-20 mol% boron oxide. The addition is boron oxide allows sintering of the composition at 1100-1200°C in 1 hour (computer translation).

It would have been obvious to one of ordinary skill in the art to have modified the method of the references as combined by also providing boron oxide (boron compound) in the mixture with the barium compound, titanium compound and nickel compound to be calcined, as taught by JP '033, to lower the sintering temperature of barium titanate semiconductor composition and to provide particle growth of uniform particle size by liquid phase sintering. Providing the boron oxide in an amount in the range of 0.2-20 mol%, as claimed in Claim 7, would have been obvious to one of ordinary skill in the art, as JP '033 teaches to provide boron oxide so that the calcined composition contains 0.3-20 mol% boron oxide.

Performing the baking at a temperature in the range of 900-1300°C for 0.5-5 hours, as claimed in Claim 22, would have been obvious to one of ordinary skill in the art, as JP '033 teaches that by providing boron oxide, the semiconductor composition can be sintered at 1100-1200°C in 1 hour.

(4)

Claims 5, 14-16, 20, 21, 23, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 6-151103 in view of either JP 63-312616 Abstract or JP 62-229602 Abstract.

JP 6-151103 discloses a method of making a laminated semiconductor constituent having positive resistance temperature comprising: forming a mixture including $BaCO_3$ (barium compound) and TiO_2 (titanium compound); baking to form a semiconductive barium titanate powder; forming semiconductor ceramic layers from slurry containing the powder; applying nickel-Pd paste on the ceramic layers to form internal electrodes; laminating the ceramic layers; baking in a reducing atmosphere; re-oxidizing; and forming external electrodes on the sintered body (computer translation). JP 6-151103 does not disclose providing a nickel compound in the mixture to be baked (calcined) to form the semiconductive barium titanate powder.

JP 63-312616 Abstract teaches that a barium titanate semiconductor composition which exhibits excellent nonlinearity and positive temperature coefficient contains as a third ingredient 0.005 – 1.5 mol% of at least one of ZnO, MnO, CoO, NiO, SnO_2 or Cr_2O_3.

JP 62-229602 Abstract teaches that a barium titanate composition for a reduction-oxidation type semiconductor capacitor of large capacity, high reliability and good temperature characteristics comprises 0.1-0.7 wt% Ni as NiO.

It would have been obvious to one of ordinary skill in the art to have modified the method of JP '103 for making a laminated barium titanate semiconductor constituent by also providing nickel oxide (nickel compound) in the mixture with the barium compound and titanium compound to be calcined to form the powder, as taught by either JP '616 or JP '602, as an ingredient that can also be provided in barium titanate semiconductor composition which exhibits excellent nonlinearity and positive temperature coefficient or which results in a reduction-oxidation type semiconductor capacitor of large capacity, high reliability and good temperature characteristics. Providing nickel oxide in a barium titanate semiconductor composition would have been obvious to one of ordinary skill in the art, as taught by either JP '616 or JP '602.

Providing the nickel oxide in an amount in the range of up to 0.2 mol%, as claimed in Claim 14, would have been obvious to one of ordinary skill in the art, as JP '616 teaches providing nickel oxide in the range of 0.005-1.5 mol%, while JP '602 teaches providing nickel oxide in the range of 0.1-0.7 wt%.

(5)

Claims 6-13, 17-19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the references as applied to claim 5 above, and further in view of JP 11-12033.

JP 11-12033 teaches that boron oxide is added to barium titanate semiconductor composition to lower the sintering temperature of the composition and to provide particle growth of uniform particle size by liquid phase sintering. Boron oxide is added to the BaCO3 and TiO2 before calcining so that the calcined composition contains 0.3-20 mol% boron oxide. The

addition is boron oxide allows sintering of the composition at 1100-1200°C in 1 hour (computer translation).

It would have been obvious to one of ordinary skill in the art to have modified the method of the references as combined by also providing boron oxide (boron compound) in the mixture with the barium compound, titanium compound and nickel compound to be calcined, as taught by JP '033, to lower the sintering temperature of barium titanate semiconductor composition and to provide particle growth of uniform particle size by liquid phase sintering. Providing the boron oxide in an amount in the range of 0.2-20 mol%, as claimed in Claim 7, would have been obvious to one of ordinary skill in the art, as JP '033 teaches to provide boron oxide so that the calcined composition contains 0.3-20 mol% boron oxide.

Performing the baking at a temperature in the range of 900-1300°C for 0.5-5 hours, as claimed in Claim 22, would have been obvious to one of ordinary skill in the art, as JP '033 teaches that by providing boron oxide, the semiconductor composition can be sintered at 1100-1200°C in 1 hour.

(6)

Claims 5 and 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno et al. 5,166,759 in view of Dirstine 4,386,985.

Ueno et al. 5,166,759 disclose a method of making a semiconductor-type laminated capacitor comprising: forming a mixture including BaO or $BaCO_3$ (barium compound) and TiO_2 (titanium compound); calcining the mixture to make a semiconductive powder; forming a raw sheet from the powder; printing inner electrode such as of nickel on the raw sheet; laminating raw sheets; sintering in a reducing atmosphere at 1200-1350°C; re-oxidizing in air; and providing

outer electrodes connected to the inner electrodes (col. 6, lines 6-66, col. 23, lines 5-54). Ueno et al. do not disclose providing a nickel compound in the mixture to be calcined to form the semiconductive powder.

Dirstine teach that in manufacturing a ceramic capacitor from a barium titanate composition and nickel electrodes, the addition of nickel oxide to the composition optimizes the dielectric properties, in particular the room temperature dielectric constant, and maintains the integrity of the nickel electrodes co-fired with the green ceramic by preventing dissolution and degradation of the nickel electrodes. The nickel oxide (NiO) is added to the composition by mixing with the $BaCO_3$ and TiO_2 and calcining (col. 3, lines 29-40, col. 8, line 26 – col. 9, line 22).

It would have been obvious to one of ordinary skill in the art to have modified the method of Ueno et a. for making a laminated barium titanate semiconductor capacitor having nickel internal electrodes by also providing nickel oxide (nickel compound) in the mixture with the barium compound and titanium compound to be calcined to form the powder, as taught by Dirstine, to optimize the dielectric properties, in particular the room temperature dielectric constant, and to maintain the integrity of the nickel electrodes co-fired with the green ceramic by preventing dissolution and degradation of the nickel electrodes.

Conclusion

(7)

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The references disclose methods of making laminated semiconductor elements.

Various references disclose including nickel, nickel oxide, boron oxide or boron nitride in barium titanate compositions.

(8)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melvin Curtis Mayes whose telephone number is 571-272-1234. The examiner can normally be reached on Mon-Fri 7:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on 571-272-1226. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Melvin Curtis Mayes
Primary Examiner
Art Unit 1734

MCM
May 27, 2004